REGEIVED
CENTRAL FAX CENTER

AUG 0 3 2009

APPLICANT(S): SERIAL NO.:

SHAHAR ATIR 10/826,375 04/19/2004

FILED: Page 2

AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

- 1. (Currently amended) A method of reading data in a virtual ground array of memory cells comprising: sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path <u>including a common sense amplifier</u>, wherein sensing includes applying a first voltage to a common word line and a substantially similar voltage to <u>source side bitlines of the cells</u> either a shared bit line or to non-shared bit lines.
- 2. (Original) The method of claim 1, wherein said sensing substantially simultaneously comprises: coupling a sense amplifier to a first source/drain terminal of each cell of said adjacent memory cells; setting a voltage at a second drain/source terminal of each cell of said adjacent cells to a read level; and sensing in a reading direction the state of said adjacent cells.
- 3. (Original) The method according to claim 1, wherein said adjacent cells share at least a word line.
- 4. (Original) The method according to claim 1, wherein said adjacent cells share at least an inside bit line.
- 5. (Currently amended) The method according to claim [[1]] 2, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier to a shared bit line of said adjacent cells.
- 6. (Currently amended) The method according to claim [[1]] 2, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier to bit lines of said adjacent cells that are not shared by said adjacent cells.

APPLICANT(S):

SHAHAR ATIR

SERIAL NO.: FILED:

10/826,375 04/19/2004

Page 3

- 7. (Original) The method according to claim 1, wherein any one of said memory cells stores at least one bit in said charge trapping region.
- 8. (Original) The method according to claim 1, wherein said adjacent cells are sensed with substantially identical current.
- 9. (Original) The method according to claim 1, wherein said memory cells are nitride read only memory (NROM) cells.
- 10. (Currently amended) The method according to claim [[1]] 2, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier through select transistors to said shared or not shared bit lines.
- 11. (Currently amended) The method according to claim [[1]] 2, wherein said coupling a sense amplifier to a first source/drain further comprising coupling said sense amplifier substantially directly to said not shared bit lines.

12. - 17. (Withdrawn)